PMC-SIERRA

PM4390
ARROW M8xFE

Advance

8 Channel 10/100 Ethernet over SONET/SDH Mapping Device

FEATURES

- Maps up to eight channels of full duplex 10/100M Ethernet into 155/622 Mbit/s SONET/SDH.
- Maps one channelized Gigabit Ethernet into 155/622 Mbit/s SONET/SDH.
- Supports packet multiplexing capabilities enabling integrated GE grooming and 10/100 port aggregation.
- Supports per port policing and rate limiting in increments of 64Kbit/s.
- Supports insertion and extraction of 802.3ah Ethernet OAM packets.
- Flexible Ethernet header filtering for VLAN & Martini MPLS support. Enabling MPLS Label Edge Router (LER) function.
- Supports multiple encapsulation protocols for worldwide interoperability including GFP-F, LAPS & flexible HDLC.
- Performs virtual and contiguous concatenation according to ITU-T G.707 and ANSI T1.105.
- Supports selection of STS-1/VC-3 virtual concatenation, VT1.5/VC-12 virtual concatenation or STS-3c /VC-4 on a per port basis.
- Generates and terminates High-Order and Low-Order SONET/SDH POH.
- Supports bandwidth provisioning in arbitrary steps of 1.6 Mbit/s (VT1.5) or 2.2 Mbit/s (VC-12).
- Supports fully integrated hitless Link Capacity Adjustment Scheme (LCAS).
- Supports up to 64 ms of differential delay.

ETHERNET SUBSYSTEM

- Provides integrated IEEE 802.3 compliant media access controllers (MAC) with per port Ethernet statistics.
- Provides IEEE 802.3 compliant Ethernet management interface (MDIO).
- Supports interfacing to full duplex 10/100M connections via SMII or SS-SMII or single GE via GMII.
- Supports loss-less IEEE 802.3 local flow-control.
- Supports frame delineation and generation with configurable IPG, preamble and CRC.
- Supports flexible Ethernet header multiplexing to enable grooming and aggregation (VLAN / MPLS / MAC) for tagged Ethernet frames.
- Supports insertion and extraction of 802.3ah Ethernet OAM packets.
- Supports frame sizes of 64 bytes to 9632 bytes with programmable frame truncation from1518 bytes to 9632 bytes.
- Supports programmable depth full packet store-and-forward buffers for burst tolerance and rate adaptation.
- Supports up to 512 Kbytes ingress buffering and 23 Kbytes of egress buffering per port.

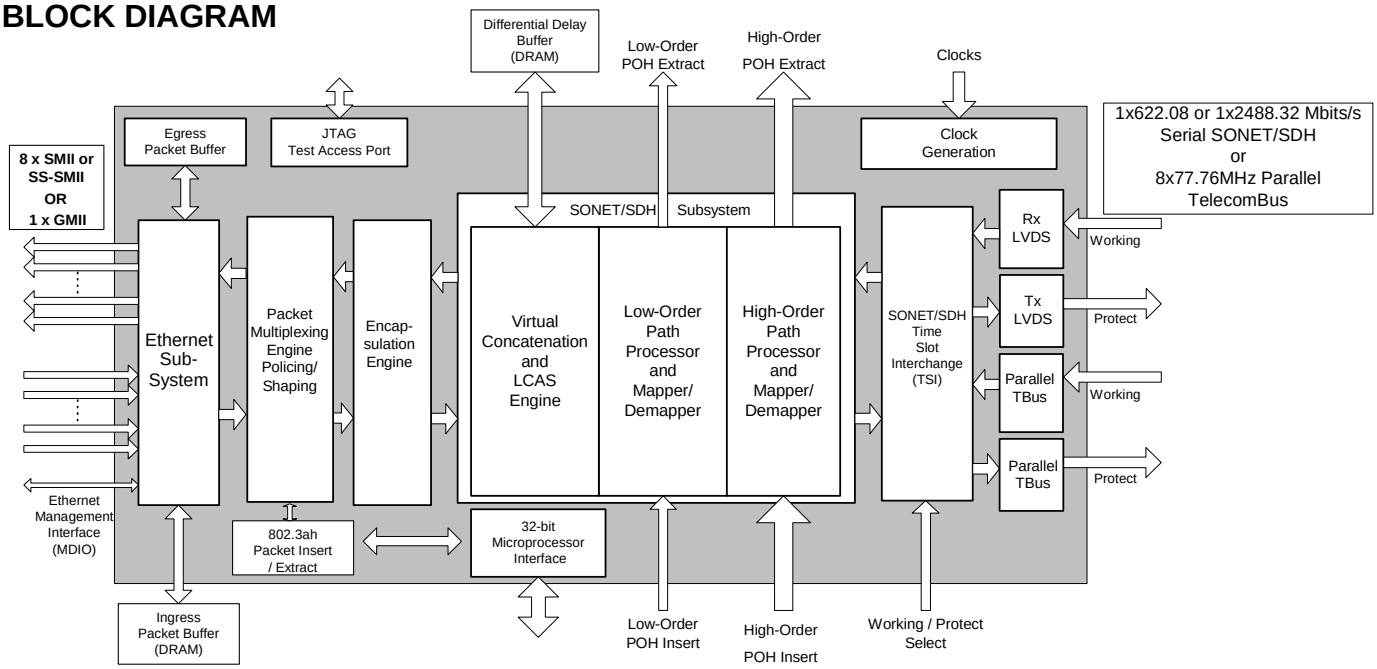
ENCAPSULATION

- Supports the following encapsulation protocols on a per port basis:
  - ITU-T G.7041 Generic Framing Procedure (GFP-F).
  - ITU-T X.86 Link Access Procedure for SDH (LAPS).
  - Flexible HDLC.
- Supports insertion and extraction of GFP Client Management Frames (CMF).
- Supports insertion and extraction of LCP, NCP and BCP control frames.

SONET/SDH SUBSYSTEM

- Supports upto 8 virtual concatenation groups (VCGs).
- Supports aggregation of all 8x10/100M ports in either of the 8 VCGs or all 8 ports into one VCG.
- Supports mapping of GE port into one VCG.

BLOCK DIAGRAM



Note: Ingress Packet Buffer and Differential Delay Buffer share the same physical memory interface.

8 Channel 10/100 Ethernet over SONET/SDH Mapping Device

- Supports grooming of GE port up to 8 VCGs.
- Supports High-Order (STS-1-Xv/VC-3-Xv & STS-3c-Xv/VC-4-Xv) and Low-Order (VT1.5-Xv/VC-12-Xv) virtual concatenation
- Supports STS-1/STM-0, STS-3c/STM-1, STS-12c/STM-4 contiguous concatenation
- Supports High-Order POH processing and pointer interpretation for STS-1, STS-3c, STS-12c, AU-3 and AU-4, AU-4-4c.
- Supports Low-Order POH processing and pointer interpretation for VT1.5, TU-12 and TU-3.
- Provides on-chip data and clock recovery and clock synthesis for SONET/SDH interfaces.
- Supports High-Order and Low Order POH insertion and extraction.
- Supports the following mapping formats:
  - C-12/ VC-12/ TU-12/ TUG-2/ TUG-3/ VC-4/ AU-4/ STM-1.
  - C-12/ VC-12/ TU-12/ TUG-2/ VC-3/AU-3/ STM-1.
  - C-3/ VC-3/ TU-3/ TUG-3/ VC-4/ AU-4/ STM-1.
  - C-3/ VC-3/ AU-3/ STM-1.
  - C-4/ VC-4/ AU-4/ STM-1.
  - VT1.5 SPE/ VT1.5/ STS-1 SPE/ STS-1.
  - STS-1 SPE/ STS-1.
  - STS-3c SPE/ STS-3c / STS-12c
- Supports LCAS according to ITU-T G.7042.
- Provides per-serial link PRBS generation and detection.
- Integrated SONET/SDH Timeslot Interchange (TSI)
  - STS-1/AU-3 granular during SONET/SDH (AU-3) operation.
  - AU-4 granular during SDH (AU-4) operation.

GENERAL

- Provides SMII/SS-SMII and GMII interfaces for connection to external Ethernet PHYs.
- Provides an MII Ethernet Management Interface (MDIO) for control and configuration of external Ethernet PHYs.
- Provides working and protect LVDS compatible WAN interfaces:
  - Multi-drop 8 x 77.76 MHz parallel TelecomBus Interface
  - 622.08 Mbit/s or 2488.32 Mbit/s SONET/SDH Serial Interface
- Provides a general purpose 32-bit µP for configuration, management and statistics gathering.
- Provides an IEEE 1149.1 compliant JTAG test port for boundary scan.

PACKAGING

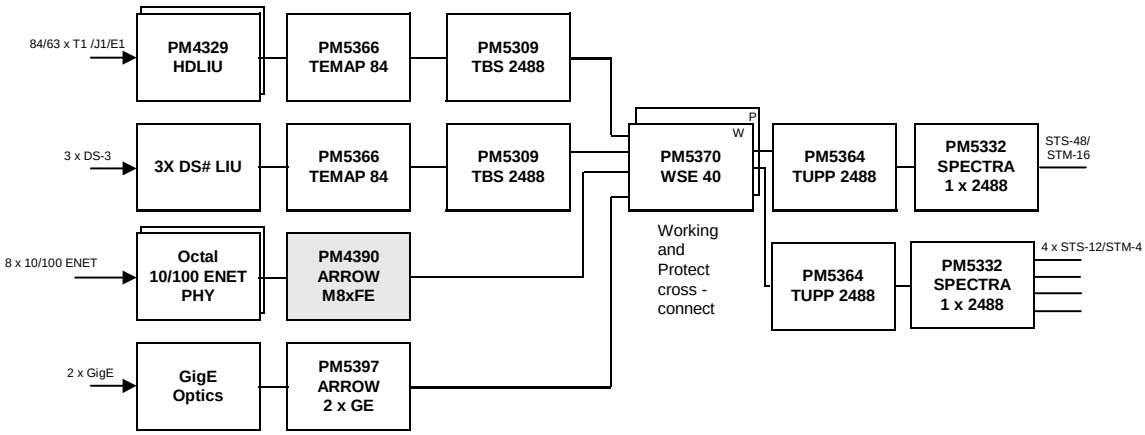
- Low power 1.2 V core with 2.5/ 3.3 V CMOS/ TTL I/O, 2.5 V SSTL_2 digital I/O.
- 31 x 31 mm 896 ball FCBGA package.
- Industrial temperature range (-40 °C to +85 °C).

APPLICATIONS

- Access and Metro Ethernet Add-Drop Multiplexers (ADM).
- Multi-service Provisioning Platforms (MSPP).
- Terminal Multiplexers.
- Next-Generation Ethernet Switches.

TYPICAL APPLICATIONS

MULTI SERVICE ADD-DROP MULTIPLEXER (USING VT/TU CROSS CONNECT)



ETHERNET TERMINAL MUX

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