Vishay Siliconix

N-Channel 100 V (D-S) MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	100			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0048			
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5 \text{ V}$	0.0070			
Q _g typ. (nC)	42			
I _D (A)	93.6			
Configuration	Single			

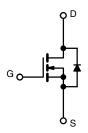
FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low R_{DS} Q_q figure-of-merit (FOM)
- Tuned for the lowest R_{DS} Q_{oss} FOM
- 100 % R_a and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

RoHS COMPLIANT HALOGEN FREE

APPLICATIONS

- · Synchronous rectification
- · Primary side switch
- DC/DC converters
- OR-ing
- Power supplies
- Motor drive control
- Battery and load switch



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR668ADP-T1-RE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	100	V	
Gate-source voltage		V _{GS}	± 20	v	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		93.6		
	T _C = 70 °C	1 , 🗔	74.8		
	T _A = 25 °C	I _D	22.9 ^{b, c}		
	T _A = 70 °C		18.3 ^{b, c}		
Pulsed drain current (t = 100 μs)		I _{DM}	200	A	
Continuous source-drain diode current	T _C = 25 °C		93.6		
	T _A = 25 °C	l _S	5.6 ^{b, c}		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	35		
Single pulse avalanche energy	L=U.I IIIH	E _{AS}	61.2	mJ	
Maximum power dissipation	T _C = 25 °C		104		
	T _C = 70 °C		66.6	w	
	T _A = 25 °C	P _D	6.25 ^{b, c}	VV	
	T _A = 70 °C		4 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) c			260		

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient b	t ≤ 10 s	R_{thJA}	15	20	°C/W		
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.9	1.2]		

Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 54 °C/W
- g. $T_C = 25$ °C

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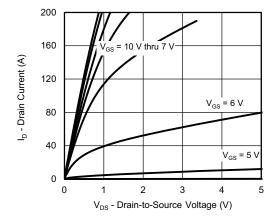
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•				
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 10 mA	-	58	-	mV/°C	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-9	-		
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	-	4	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	100	nA	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V	-	-	1	μА	
		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15		
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40	-	-	Α	
Duning and the second of the s	Б	V _{GS} =10 V, I _D = 20 A	-	0.0040	0.0048		
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 7.5 V, I _D = 15 A	-	0.0054	0.0070	Ω	
Forward transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A	-	85	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	3750	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	395	-		
Reverse transfer capacitance	C _{rss}		-	18	-		
Tatal asta shaws	0	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	-	54	81	nC	
Total gate charge	Qg		-	42	63		
Gate-source charge	Q _{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 7.5 \text{ V}, I_D = 10 \text{ A}$	-	17.5	-		
Gate-drain charge	Q _{gd}		-	11.4	-		
Output charge	Q _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	73	-		
Gate resistance	R_g	f = 1 MHz	0.3	0.9	1.6	Ω	
Turn-on delay time	t _{d(on)}		-	21	42		
Rise time	t _r	$V_{DD} = 50 \text{ V}, R_1 = 5 \Omega, I_D \cong 10 \text{ A},$	-	18	36		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	36	72		
Fall time	t _f		-	10	20		
Turn-on delay time	t _{d(on)}		-	25	50	ns	
Rise time	t _r	V_{DD} = 50 V, R_L = 5 Ω , I_D \cong 10 A,	-	61	122		
Turn-off delay time	t _{d(off)}	$V_{GEN} = 7.5 \text{ V}, R_g = 1 \Omega$	-	34	68		
Fall time	t _f		-	11	22		
Drain-Source Body Diode Characteristi	cs						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	93.6	٨	
Pulse diode forward current	I _{SM}		-	-	200	A	
Body diode voltage	V_{SD}	I _S = 5 A, V _{GS} = 0 V	-	0.73	1.1	٧	
Body diode reverse recovery time	t _{rr}		-	59	118	ns	
Body diode reverse recovery charge	Q _{rr}	1 10 A di/dt 100 A/v- T 05 00	-	115	230	nC	
Reverse recovery fall time	ta	$I_F = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$	-	41	-		
Reverse recovery rise time	t _b		-	18	-	ns	

Notes

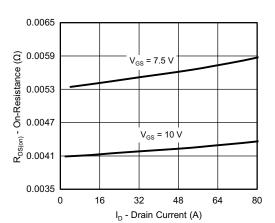
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

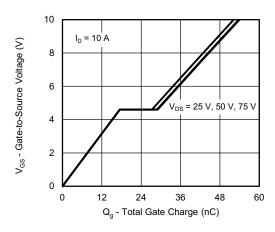




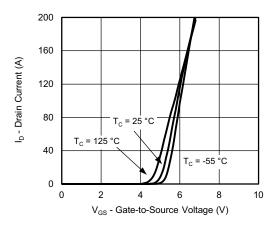
Output Characteristics



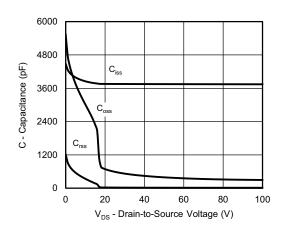
On-Resistance vs. Drain Current and Gate Voltage



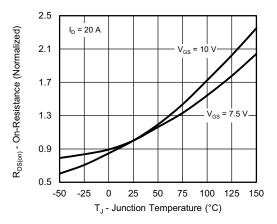
Gate Charge



Transfer Characteristics

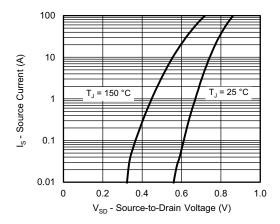


Capacitance

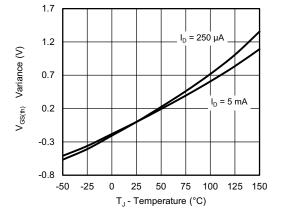


On-Resistance vs. Junction Temperature

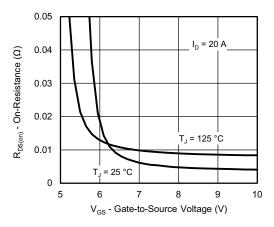




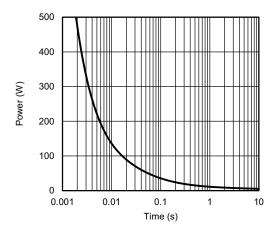
Source-Drain Diode Forward Voltage



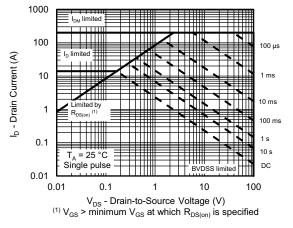
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

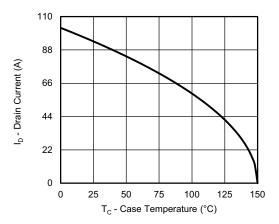


Single Pulse Power, Junction-to-Ambient

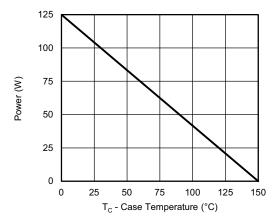


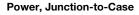
Safe Operating Area, Junction-to-Ambient

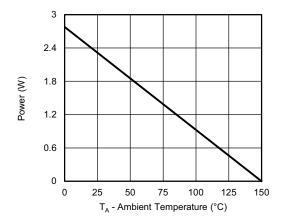




Current Derating a





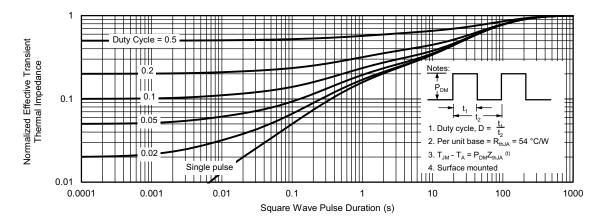


Power, Junction-to-Ambient

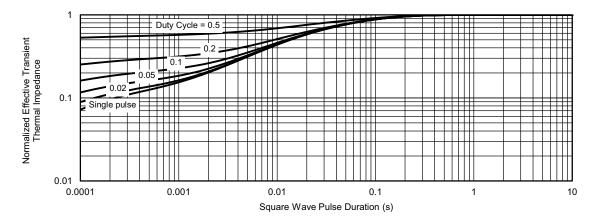
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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