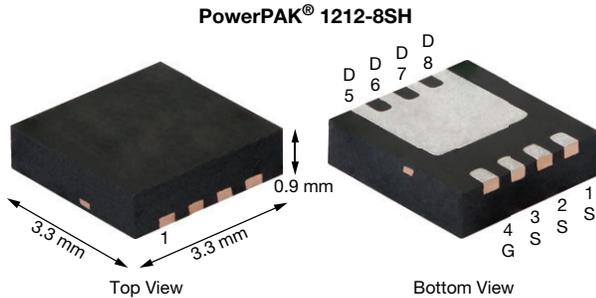


## P-Channel 30 V (D-S) MOSFET



PRODUCT SUMMARY	
$V_{DS}$ (V)	-30
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -10$ V	0.0123
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.0222
$Q_g$ typ. (nC)	20.5
$I_D$ (A) <sup>d, g</sup>	-35
Configuration	Single

### FEATURES

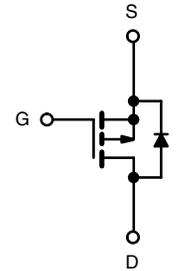
- TrenchFET<sup>®</sup> power MOSFET
- 100 %  $R_g$  and UIS tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Notebook battery charging
- Notebook adapter switch



P-Channel MOSFET

### ORDERING INFORMATION

Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH617DN-T1-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	-30	V
Gate-source voltage	$V_{GS}$	$\pm 25$	V
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	-35 <sup>d</sup>
		$T_C = 70$ °C	-35 <sup>d</sup>
		$T_A = 25$ °C	-13.9 <sup>a, b</sup>
		$T_A = 70$ °C	-11.1 <sup>a, b</sup>
Pulsed drain current	$I_{DM}$	-60	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	-35 <sup>d</sup>
		$T_A = 25$ °C	-3 <sup>a, b</sup>
Avalanche current	$I_{AS}$	-29	A
Single-pulse avalanche energy	$E_{AS}$	42	mJ
Maximum power dissipation	$P_D$	$T_C = 25$ °C	52
		$T_C = 70$ °C	33
		$T_A = 25$ °C	3.7 <sup>a, b</sup>
		$T_A = 70$ °C	2.4 <sup>a, b</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>e, f</sup>		260	°C

### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>a, c</sup>	$R_{thJA}$	26	33	°C/W
Maximum junction-to-case	$R_{thJC}$	1.9	2.4	

#### Notes

- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- Maximum under steady state conditions is 81 °C/W
- Package limited
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Based on  $T_C = 25$  °C



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$	-	-25	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	4.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1.2	-	-2.5	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	-5	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq -10\text{ V}, V_{GS} = -10\text{ V}$	-30	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -13.9\text{ A}$	-	0.0103	0.0123	$\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -10.3\text{ A}$	-	0.0185	0.0222	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -13.9\text{ A}$	-	35	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1800	-	pF
Output capacitance	$C_{oss}$		-	370	-	
Reverse transfer capacitance	$C_{rss}$		-	312	-	
Total gate charge	$Q_g$	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -13.9\text{ A}$	-	39	59	nC
		$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -13.9\text{ A}$	-	20.5	31	
Gate-source charge	$Q_{gs}$	$V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -13.9\text{ A}$	-	6	-	
Gate-drain charge	$Q_{gd}$		-	11	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.4	2	4	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.35\text{ }\Omega$ $I_D \cong -11.1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$	-	11	22	ns
Rise time	$t_r$		-	9	18	
Turn-off delay time	$t_{d(off)}$		-	32	50	
Fall time	$t_f$		-	9	18	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.35\text{ }\Omega$ $I_D \cong -11.1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	-	40	60	ns
Rise time	$t_r$		-	43	65	
Turn-off delay time	$t_{d(off)}$		-	30	45	
Fall time	$t_f$		-	11	22	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	-35	A
Pulse diode forward current	$I_{SM}$		-	-	-60	
Body diode voltage	$V_{SD}$	$I_S = -11.1\text{ A}, V_{GS} = 0\text{ V}$	-	-0.8	-1.2	V
Body diode reverse recovery time	$t_{rr}$	$I_F = -11.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	33	50	ns
Body diode reverse recovery charge	$Q_{rr}$		-	30	45	nC
Reverse recovery fall time	$t_a$		-	18	-	ns
Reverse recovery rise time	$t_b$		-	16	-	

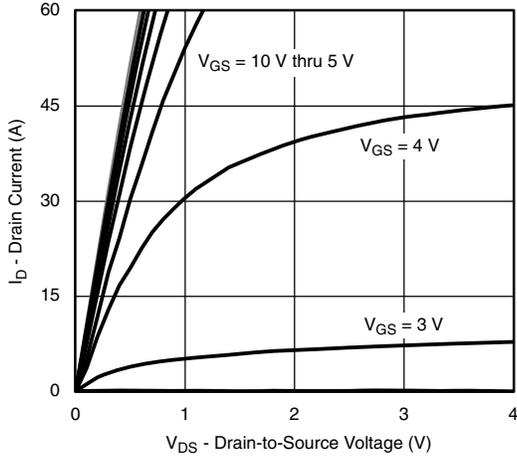
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

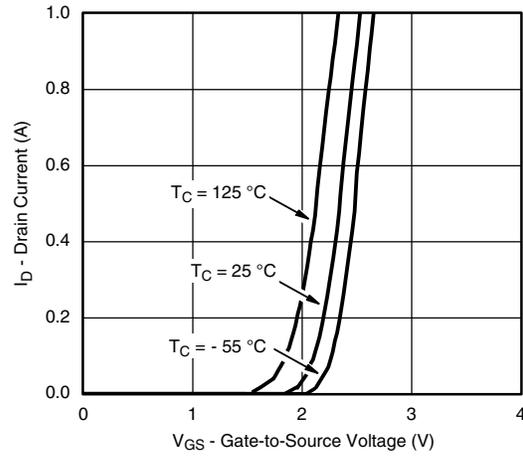
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



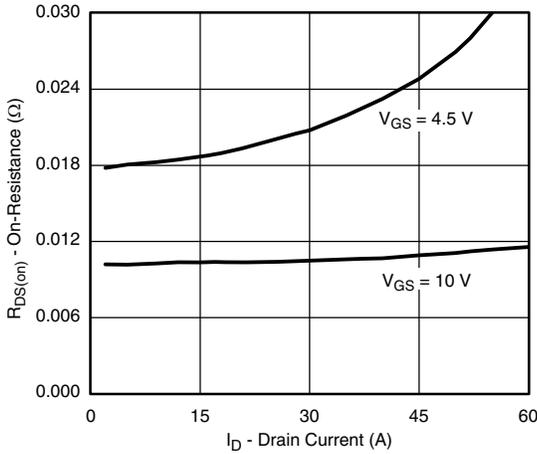
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



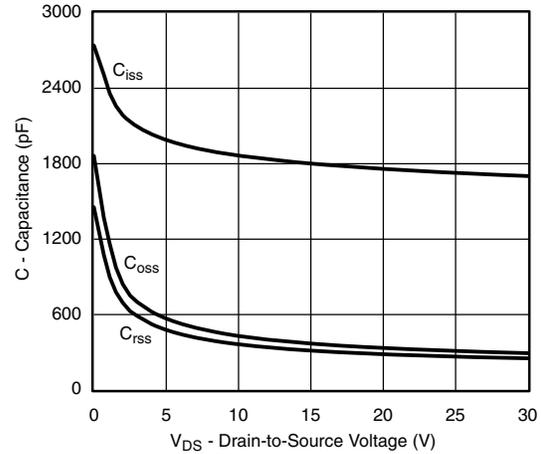
Output Characteristics



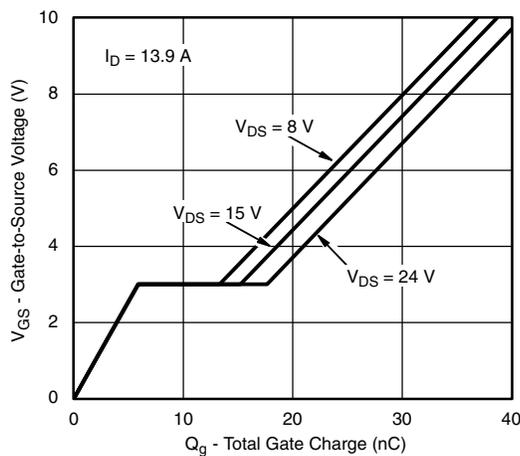
Transfer Characteristics



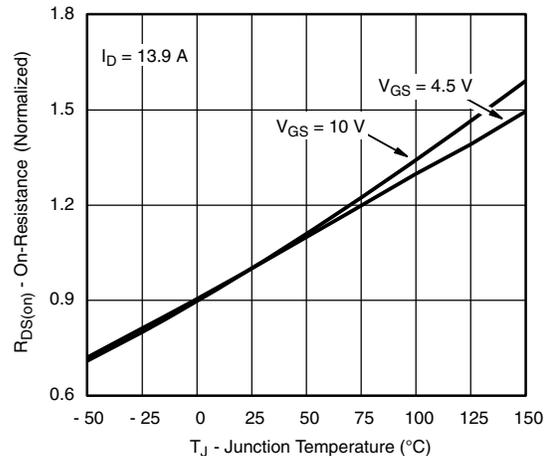
On-Resistance vs. Drain Current



Capacitance



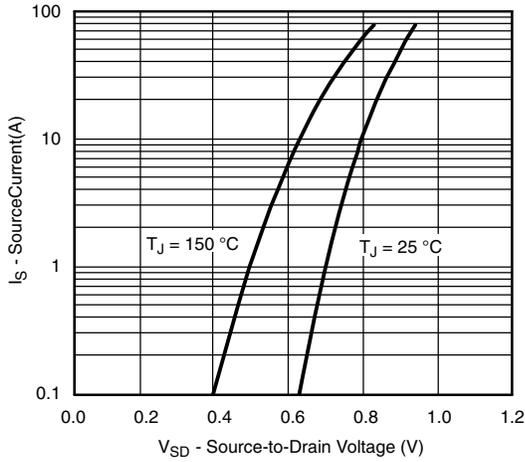
Gate Charge



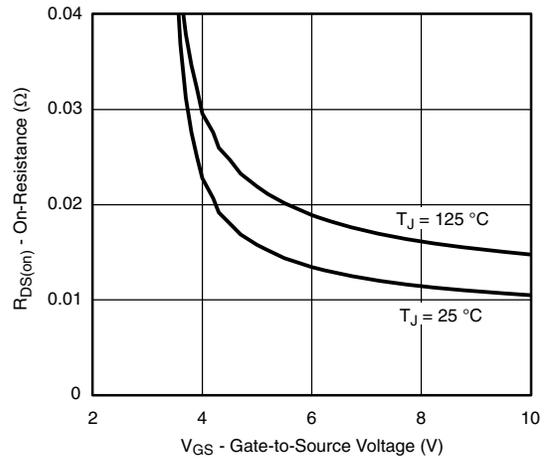
On-Resistance vs. Junction Temperature



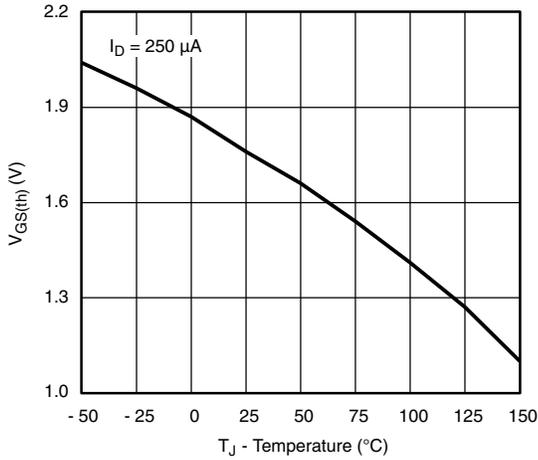
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



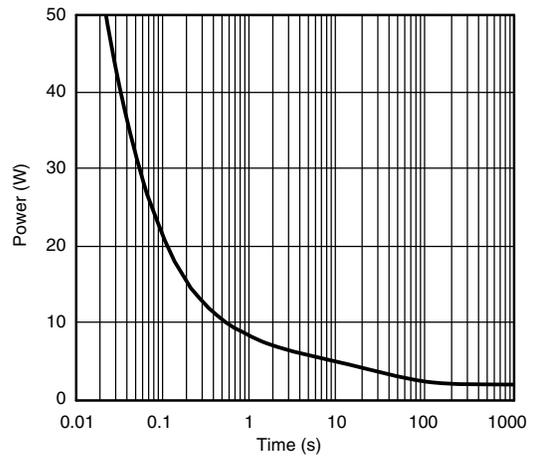
Source-Drain Diode Forward Voltage



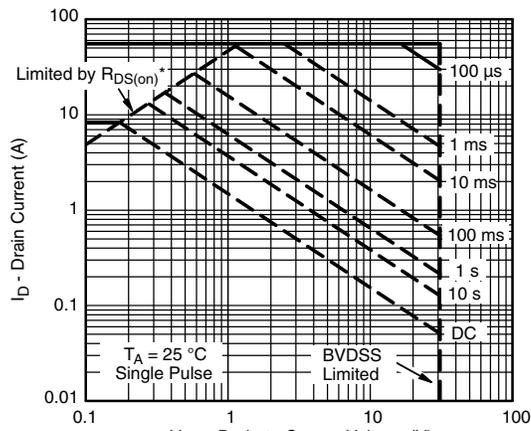
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



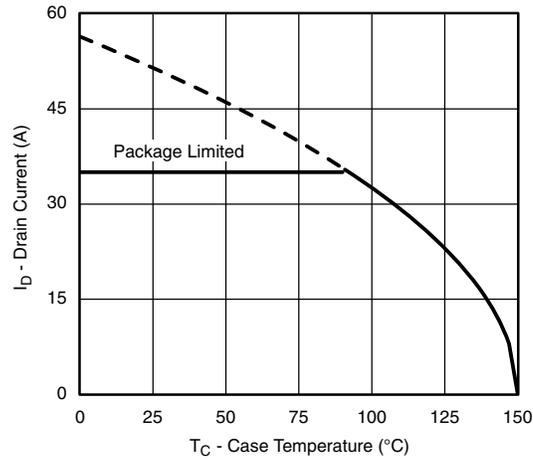
Single Pulse Power, Junction-to-Ambient



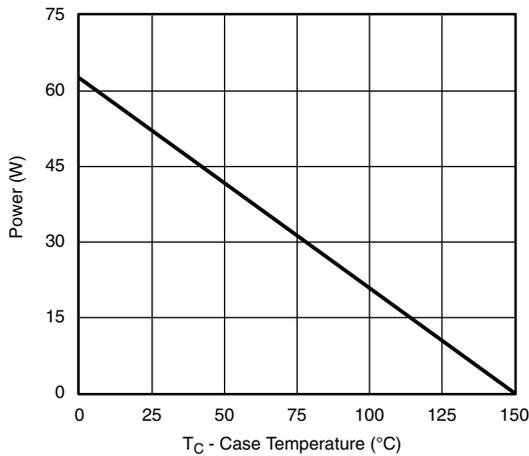
Safe Operating Area



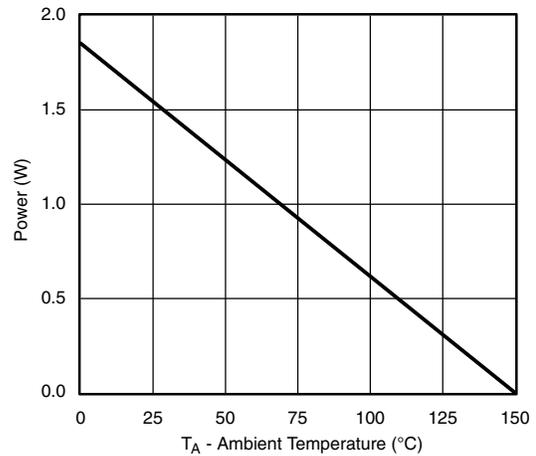
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating<sup>a</sup>**



**Power Derating, Junction-to-Case**



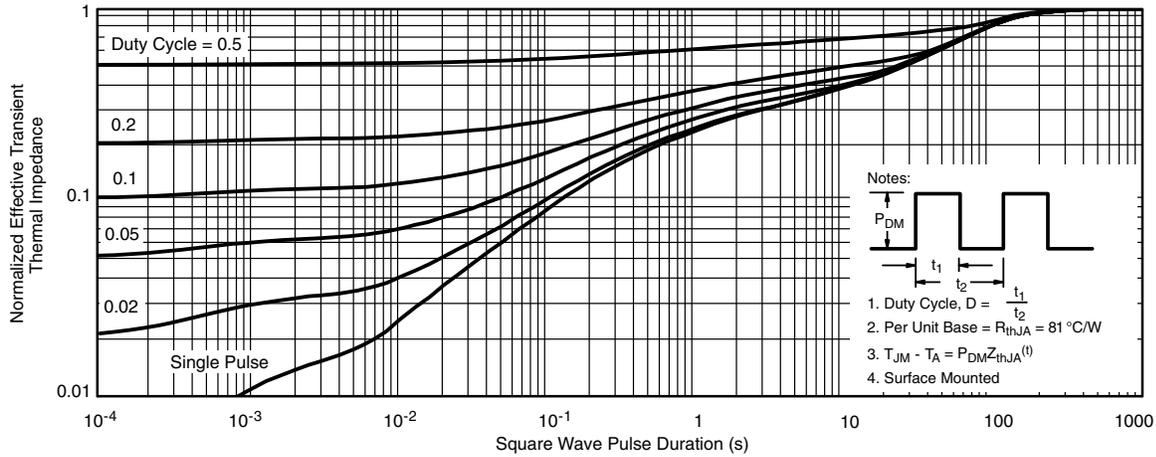
**Power Derating, Junction-to-Ambient**

**Note**

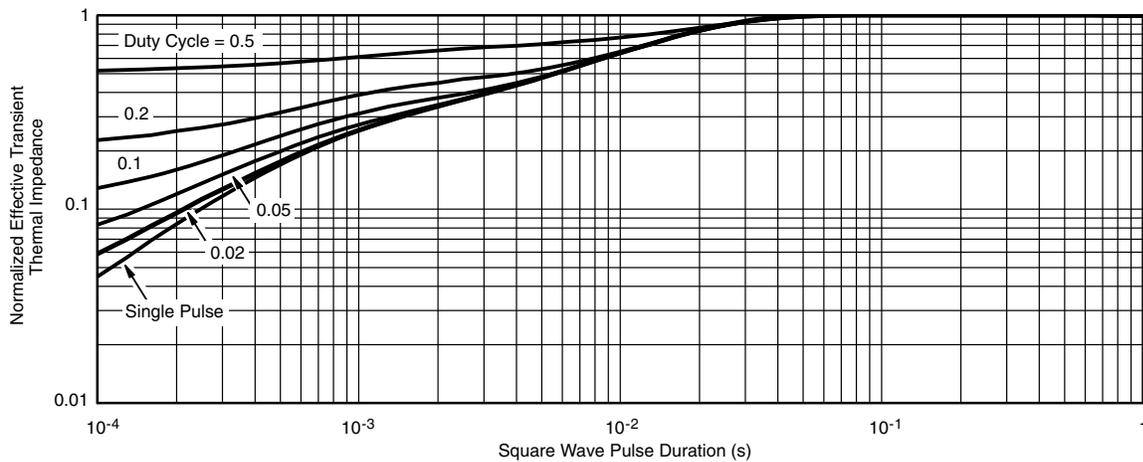
- a. The power dissipation  $P_D$  is based on  $T_J$  max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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